The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No.15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte FERNANDO GONZALEZ and DAVID KAO

Appeal No. 2001-1549
Application No. 09/375,081

ON BRIEF

Before JERRY SMITH, DIXON, and BLANKENSHIP, **Administrative Patent Judges**.

DIXON, **Administrative Patent Judge**.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 15-19 and 23, which are all of the claims pending in this application.

We AFFIRM.

Appellants' invention relates to transistors having controlled conductive spacers which act as additional gates for a single transistor, uses of such transistors and methods of making such transistors. An understanding of the invention can be derived from a reading of exemplary claim 15, which is reproduced below.

15. A multiple gate transistor structure comprising:

a gate structure formed on a first oxide layer on a semiconductor structure and defining a first gate;

a secondary oxide layer formed over said gate structure;

a spacer formed on at least one side of said gate structure on said secondary oxide layer, at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate;

a first contact to said gate structure; and

at least a second contact to said conductive portion of said spacer.

The prior art of record relied upon by the examiner in rejecting the appealed claims are as follows:

Rao (Rao '139)	4,213,139	Jul. 15, 1980
Rao (Rao '263)	4,319,263	Mar. 9, 1982

Claims 15, 17, 19, and 23 stand rejected under 35 U.S.C. § 102 as being anticipated by Rao '139. Claims 15-19 and 23 stand rejected under 35 U.S.C. § 102 as being anticipated by Rao '263.[1]

Rather than reiterate the conflicting viewpoints advanced by the examiner and appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 11, mailed Aug. 25, 2000) for the examiner's reasoning in support of the rejections, and to appellants' brief (Paper No. 8, filed May 15, 2000) and reply brief (Paper No. 13, filed Oct. 13, 2000) for appellants' arguments thereagainst.

OPINION

In reaching our decision in this appeal, we have given careful consideration to appellants' specification and claims, to the applied prior art references, and to the respective positions articulated by appellants and the examiner. As a consequence of our review, we make the determinations which follow.

At the outset, we note that appellants have elected to group all the claims as standing or falling together. (See brief at page 4.) Therefore, we select independent claim 15 as the representative claim and address appellants' arguments thereto with respect to Rao '263 since the examiner applies this reference against all the pending claims.

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[1] After appellants filed a terminal disclaimer, the examiner withdrew the rejection under obvious-type double patenting.

"Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention." **RCA Corp. v. Applied Digital Data Systems. Inc.**, 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984).

It is well settled that the burden of establishing a ***prima facie*** case of anticipation resides with the Patent and Trademark Office (PTO). **See In re Piasecki**, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984). After the PTO establishes a ***prima facie*** case of anticipation based on inherency, the burden shifts to the appellants to prove that the subject matter shown to be in the prior art does not possess the characteristics of the claimed invention. **See In re Thorpe**, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985); **In re King**, 801 F.2d 1324, 1327, 231 USPQ 136, 138 (Fed. Cir. 1986). Hence, appellants' burden before the PTO is to prove that the applied prior art reference does not perform the functions defined in the claims. Compare **In re Best**, 562 F.2d 1252, 1255, 195 USPQ 430, 433-34 (CCPA 1977); **In re Ludtke**, 441 F.2d 660, 664, 169 USPQ 563, 566-67 (CCPA 1971). The examiner maintains that Rao '139 teaches "a multiple gate transistor structure" as recited in the language of independent claim 15. (See answer at pages 4-5.) Additionally, the examiner maintains that the two gate transistor may be represented by an equivalent circuit of two transistors as in Figure 2 and the three gate transistor may be

represented by an equivalent circuit of three transistors as in Figure 7. The examiner maintains that the multigate transistor of the present invention may be represented by three transistors as shown in Figures 5 and 6. We agree with the examiner and find that the examiner has established a ***prima facie*** case of anticipation.

Appellants argue that the examiner has not established a ***prima facie*** case of anticipation since Rao '139 is directed to a pair of transistors where each of the transistors has exactly one gate. Additionally, Rao '263 discloses a plurality of transistors formed with adjacent transistors which share a common source/drain region and each of the transistors has exactly one gate. Appellants argue that the claimed invention relates to a multiple gate transistor structure which includes a gate spacer wherein the spacer takes the form of the second gate or second and third gates of the single transistor. (See brief at pages 7-8.) Appellants argue that "Rao '263 fails to disclose a transistor with at least a second gate." (See brief at page 8.) Here, we note that the language of independent claim 15 does not explicitly require that there be a single transistor. A "multiple gate transistor structure" is recited in claim 15. We find that the overlapping transistors of Rao '139 and '263 teach the recited limitations in independent claim 15. For example, Rao '263 teaches a gate structure (15) formed on a first oxide layer (22) on a semiconductor structure (P) and defining a first gate; a secondary oxide layer (21, 23) formed over said gate structure (15); a spacer (40) formed on at least one side of said gate structure on said secondary oxide layer

(21, 23), and at least a portion of said spacer adjacent to said secondary oxide layer being conductive and defining at least a second gate (41). Rao '263 does not expressly disclose contacts to the two gates, but it is deemed inherent that there would be contacts to allow signals to be connected thereto as shown in the schematic in Fig. 7. Additionally, Rao '263 also discloses that the insulator layers 21 and 23 are thermal silicon oxide. (Column 2, line 30.) Therefore, we find that Rao teaches the claimed invention.

Appellants argue that Rao '263 does not teach each and every element of the claimed invention. (See brief at page 8.) We disagree with appellants as discussed above. Appellants argue that Rao '263 does not teach a spacer or a conductive spacer as recited in independent claim 15. (See brief at page 8.) We disagree with appellants and find that the gate 41 may be deemed to be a conductive spacer in "a multigate transistor structure" as recited in independent claim 15.

Although appellants have elected to group all the claims together, appellants have included general (non-specific) arguments to all claims and relies on the arguments made with respect to independent claim 15. Generally, appellants' arguments are that Rao '139 and '263 are directed to plural transistors. While we agree that both Rao references teach the use of plural transistors, we do not find this distinguishes over the claimed "plural gate transistor structure." We find no limitation in the language of independent claim 15 that there only be a single transistor in the

device. Nor do we find any limitation as to how the gates are used or connected to each other or to other circuitry. For example, we find no limitation that each of the gates is connected to the same/single control signal as shown in appellants' figure 5. Contrary to the requirement of a single input to the plural gates, appellants show an embodiment in Figure 6 with the plural gates connected to plural inputs. As the examiner points out at page 4 of the answer, the equivalent circuit diagram for the implementation/use of appellants' multiple gate transistor is similar to the multiple transistor equivalent circuits disclosed by Rao '139 and '263. We find no response by appellants in the reply to the examiner's correlation of the equivalent circuit schematics of the single transistor device and a multiple transistor device. Appellants merely maintain that a two and three transistor circuit fail to anticipate a single (multiple gate) transistor. Additionally, we note that the language of independent claim 15 is open ended and also recites a "structure" rather than a single transistor. Therefore, appellants' arguments to the distinction between a single transistor and multiple transistors is not persuasive.

Appellants additionally argue that spacers are semiconductor structures which are typically used in the formation of lightly doped drain (LDD) transistors and that neither Rao '139 nor Rao '263 includes the term "spacer" nor do they teach or suggest a spacer as the term is defined and understood in the art. (See brief at pages 11-12.) We do not find that appellants' specification defines the term, nor have appellants

provided any specific definition of the term "spacer." The mere fact that spacers are used in LDD devices does not thereby define the structure of a spacer to distinguish it from the gate disclosed by Rao. Furthermore, we find no limitation in the language of independent claim 15 that requires a LDD transistor. Therefore, this argument is not persuasive.

Appellants argue in the reply brief at page 2 that at least a portion of the spacer is conductive and that appellants' spacer has both conductive and non-conductive portions. We find no limitation in the language of independent claim 15 to support this argument since there is no limitation that the spacer must also be non-conductive. Lastly, appellants argue in the reply brief at page 2 that Rao '139 and Rao '263 fail to teach a first contact and a second contact. We have addressed this above as an inherent feature of Rao '139 and Rao '263 to apply the disclosed signals. Therefore, this argument is not persuasive, and we will sustain the rejection of independent claim 15 since appellants have not adequately rebutted the ***prima facie*** case of anticipation established by the examiner. Since appellants elected to group all the claims in a single group, we will similarly sustain the rejection of claims 16-19 and 23.

CONCLUSION

To summarize, the decision of the examiner to reject claims 15-19 and 23 under 35 U.S.C. § 102 is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

JERRY SMITH
Administrative Patent Judge

JOSEPH L. DIXON
Administrative Patent Judge

HOWARD B. BLANKENSHIP
Administrative Patent Judge

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) APPEALS
) AND
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